oneAPI Workshop

“Using Intel® oneAPI Toolkits with FPGAs Virtual Workshop”

15th December 2021
Introduction to Innovator Program
(https://devmesh.intel.com-> member Programs)

TOP TIER EXPERTS WHO INNOVATE & LIKE TO SHARE WORK GO UNDER NDA

ACCESS TO INTEL HARDWARE & INTEL EXPERTISE

EARLY EXPERIMENTS, PROTOTYPES, TESTING & RESEARCH

SPOTLIGHT

SPEAKERSHIPS & DEMOS AT MAJOR CONFERENCES AND PUBLIC EVENTS

- Shared Projects - Mesh
- Technical Articles
- Media Articles
- Event Demos
- Devs Trained
- Product Feedback
Intel® oneAPI Technology Partners

Companies endorsed by Intel who provide services based on their Intel® oneAPI technical expertise to meet the business and technical needs of customers and the local developer community.

Connecting with an Intel® oneAPI Technology Partner:

- 19 companies in 10 countries
- Certified on various programming models for HPC and AI using Intel oneAPI
- Find your local expert here:

PARTNER QUALIFICATIONS:

1. Expertise in parallel programming for CPU & GPU
2. Provide consulting & services such as porting applications, coding, tuning, code-modernization, etc.
3. Successful completion of training portal and technical assessments
Intel® Certified Instructors for oneAPI

Intel® Certified Instructors are endorsed by Intel to teach oneAPI topics creating a global network of oneAPI experts.

Instructors come from consulting companies & solution providers in the Intel® oneAPI Technology Partner Program, academia and the Software Innovator program.

Connecting with an Intel® Certified Instructor:

- 64 instructors certified to teach Data Parallel C++ across 10 countries
- Find your local expert here:
  - software.intel.com/oneAPI/training/certified-instructors

INSTRUCTOR QUALIFICATIONS:

1. Technical expertise and mastery of DPC++ language
2. Demonstrated teaching ability
3. Ability to use Intel® DevCloud as a teaching tool
4. Successful completion of our hands-on workshops and assessments
What’s next.....

Try your code on Intel® DevCloud
Develop, run, and optimize your oneAPI project on the Intel® DevCloud, a free development sandbox with access to the latest hardware and software from Intel. No software downloads. No configuration steps. No installations. Get started in minutes.

Continue your self-paced learning
Work step-by-step through code examples to that will help you optimize your Intel® oneAPI solution in the Intel® DevCloud and enhance your understanding of DPC++.

Innovate, Collaborate & Share on DevMesh:
Submit your project to showcase your work and get feedback and support from experts and Intel. See how others are leveraging Intel® oneAPI Products.
Intel’s community portal for developers and creators who want to share their work and best practices to the community while building a professional profile of amazing work and activities.

- Find Amazing Research and Projects. [Go to Project]
- Developer Profiles [Go to People]
- Developer Blogs [Go to Blogs]
- Project Groups [Go to Groups]
- Become A Developer Leader [Go To Members Programs]
Agenda

- Industry Trends: Heterogeneous computing
  - Cloud, Edge, Network Transformation
- Intel FPGA Roadmap
- oneAPI Ecosystem and Success Story
- Using FPGAs with the Intel® oneAPI Toolkits
  - Introduction to oneAPI
  - What are FPGAs and Why Should I Care About Programming Them?
  - Development Flow for Using FPGAs with the Intel® oneAPI Toolkits
  - Lab: Practice the FPGA Development Flow
- Optimizing Your Code for FPGAs
  - Introduction to Optimizing FPGAs with the Intel oneAPI Toolkits
  - Lab: Optimizing the Hough Transform Kernel
INCREASING WORKLOAD DIVERSITY

POWERED BY AI

DEPLOYMENTS SPANNING CLOUD, ENTERPRISE, HPC, IOT

Source: Intel forecast
WAREHOUSE SCALE COMPUTING

FEATURE ATTRIBUTES
- Virtualization & Containerization
- Quality of Service
- RAS (Reliability, Availability, Serviceability)
- Security
- Power Management

DATACENTER IS THE COMPUTER
EDGE IS THE EPICENTER OF INNOVATION

By 2022, **45%** Of Data Will Be Stored, Analyzed, And Acted On At The Edge

**Drivers for Edge**
Latency, Bandwidth, Security, Connectivity

**Orchestration Across Edge & Cloud To Deliver Use Case Metrics**
Cloudification brings:

- Intelligence where needed
- Flexibility and agility
- Single scalable architecture
- New services

**Legacy**
- Custom Proprietary
- Hardware Defined

**Modern, Cloud-ready**
- NFV + SDN Orchestration
- Software Defined
- Open Platforms
- Virtualized Containers

**Next Generation Networks**
- Network Slicing
- Analytics Core to Edge
- Visual Cloud

**5G**
Advantages of Heterogeneous Computing

Multiple Architectures

Developers can optimize specialized inline and offload workloads to meet business needs.

- Strengths of individual xPUs (CPU, GPU, FPGAs, etc.) can be combined for the benefit of the overall system.
DIVERSE WORKLOADS REQUIRE DIVERSE ARCHITECTURES

The future is a diverse mix of scalar, vector, matrix, and spatial architectures deployed in CPU, GPU, AI, FPGA and other accelerators.

Refer to software.intel.com/articles/optimization-notice for more information regarding performance & optimization choices in Intel software products.

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# FPGA Roadmap

**EMIB to Co-EMIB to Foveros**

<table>
<thead>
<tr>
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<th>Monolithic</th>
<th>EMIB (2.5D)</th>
<th>Co-EMIB / Foveros (3D)</th>
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<tbody>
<tr>
<td><strong>Arria®10</strong></td>
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<td><img src="image" alt="Production" /></td>
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<td><img src="image" alt="EMIB (2.5D)" /></td>
<td><img src="image" alt="Co-EMIB / Foveros (3D)" /></td>
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<tr>
<td><strong>Agilex™</strong></td>
<td><img src="image" alt="Sampling" /></td>
<td><img src="image" alt="2nd Gen" /></td>
<td><img src="image" alt="Co-EMIB / Foveros (3D)" /></td>
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<tr>
<td><strong>Next Gen FPGAs</strong></td>
<td><img src="image" alt="Next Gen FPGAs" /></td>
<td><img src="image" alt="2nd Gen" /></td>
<td><img src="image" alt="Co-EMIB / Foveros (3D)" /></td>
</tr>
</tbody>
</table>
**Agilex™ Performance/Power**

Based on Intel® 10nm Process

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**Agilex™ 40+% Geomean Max. Frequency Improvement over Stratix®10**

**Agilex™ Significant Speed Up**
In Data Center, Network & Edge

**Agilex™ Average 1.5x faster**
in Combinational LUT Delay

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**Intel® Agilex™ FPGAs Deliver Significantly Better Performance/Watt**

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Refer to [software.intel.com/articles/optimization-notice](software.intel.com/articles/optimization-notice) for more information regarding performance & optimization choices in Intel software products.

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FPGA-Processor Attach Chiplets

Acceleration & Efficient Processing of Diverse Workloads

- Workload Acceleration
- Standard PCIe infrastructure
- Enhanced Workload Acceleration
- Coherent Memory Customization/Expansion

Next Gen CXL + PCIe

High-bandwidth Acceleration for applications including:
- >400G networks
- Edge analytics
- Data center workloads
Intel® Stratix® 10 NX FPGA
Intel's first AI-optimized FPGA

**HIGH PERFORMANCE AI MATRIX BLOCKS**
- Up to 15X more INT8 compute performance than today's Stratix 10 MX for AI workloads
- Hardware programmable for AI with customized workloads

**ABUNDANT NEAR-COMPUTE MEMORY**
- Embedded and customizable memory hierarchy for model persistence
- Integrated HBM for high memory bandwidth

**HIGH BANDWIDTH NETWORKING**
- Up to 57.8G PAM4 transceivers and hard Intel Ethernet blocks for high efficiency
- Flexible and customizable interconnect to scale across multiple nodes

**EXTENSIBLE**
- Chiplets enable easier interface customization and ASIC extensions

Matrix Compute, Memory & Networking delivers high performance HW optimized for AI
Programming Challenges for Multiple Architectures

Growth in specialized workloads

Variety of data-centric hardware required

Separate programming models and toolchains for each architecture are required today

Software development complexity limits freedom of architectural choice
oneAPI
One Programming Model for Multiple Architectures and Vendors

Freedom to Make Your Best Choice
- Choose the best accelerated technology the software doesn’t decide for you

Realize all the Hardware Value
- Performance across CPU, GPUs, FPGAs, and other accelerators

Develop & Deploy Software with Peace of Mind
- Open industry standards provide a safe, clear path to the future
- Compatible with existing languages and programming models including C++, Python, SYCL, OpenMP, Fortran, and MPI
Open to promote community and industry collaboration

Enables code reuse across architectures and vendors

Visit oneapi.com for more details

The productive, smart path to freedom for accelerated computing from the economic and technical burdens of proprietary programming models
Intel® oneAPI Toolkits
A complete set of proven developer tools expanded from CPU to XPU

**Intel® oneAPI Base Toolkit**
Native Code Developers

A core set of high-performance tools for building C++, Data Parallel C++ applications & oneAPI library-based applications

**Add-on Domain-specific Toolkits**
Specialized Workloads

- **Intel® oneAPI Tools for HPC**
  Deliver fast Fortran, OpenMP & MPI applications that scale

- **Intel® oneAPI Tools for IoT**
  Build efficient, reliable solutions that run at network’s edge

- **Intel® oneAPI Rendering Toolkit**
  Create performant, high-fidelity visualization applications

**Toolkits powered by oneAPI**
Data Scientists & AI Developers

- **Intel® AI Analytics Toolkit**
  Accelerate machine learning & data science pipelines with optimized DL frameworks & high-performing Python libraries

- **Intel® Distribution of OpenVINO™ Toolkit**
  Deploy high performance inference & applications from edge to cloud

Latest version is 2021.1
Intel® FPGAs + Intel® oneAPI Toolkits

**Spatial Architecture**
- Data-dependent parallelism
- Streaming and graph processing patterns

**Rich I/O**
- Low and deterministic latency
- Customizable network interfaces and protocols

**Memory**
- Customizable memory architecture
- Distributed, high bandwidth, on-chip memory topology

**oneAPI Product**

**Direct Programming**

**Analysis & Debug Tools**

**Data Parallel C++**
Getting Started with oneAPI on an FPGA

Intel® oneAPI Base Toolkit + Intel® FPGA Add-on for oneAPI Base Toolkit + Board Support Package (BSP)

Note: Developers using custom platforms should download the Intel® FPGA Add-on for Intel® Custom Platforms with the respective Intel® Quartus® version and obtain a BSP from their 3rd part platform vendor.
Intel oneAPI/DPC++ Feature Update

- 100% Performance parity with OpenCL

- Custom Boards/Platforms: Intel® Quartus® Release (19.4, 20.2, 20.3)

- IO pipes/channels/streams

- Unified Shared Memory (USM): Explicit & Restricted

- High Bandwidth Memory (HBM)
FPGA Development Flow for oneAPI Projects
Intel® oneAPI Toolkits
Free Availability

Get Started Quickly
Code Samples, Quick-start Guides, Webinars, Training

software.intel.com/oneapi
Intel® oneAPI Toolkits – Proven Performance
Top Takeaways & Proof Points

- **HPC Cross-architecture** – Argonne National Labs is running Exascale-class applications efficiently on current and future generations of Intel CPUs and GPUs.

- **HPC Cross-architecture** – Zuse Institute Berlin (ZIB) ported the tsunami simulation easyWave application from CUDA to Data Parallel C++ delivering performance across multiple architectures from multiple vendors.

- **HPC & AI** – CERN uses Intel® DL Boost and oneAPI to speed simulations with inference acceleration by nearly 2x without accuracy loss*.

- **Hyper-real Visualization & AI Using Advanced Ray Tracing** – Bentley Motors Limited’s AI-based car configurator processes 1.7M+ images with up to 10B possible configurations per model*.

- **IoT** – Samsung Medison accelerates ultrasound image processing at the edge on multiple Intel® architectures for improved accuracy and fast diagnosis.

- **Major CSPs & Framework** endorse oneAPI – Microsoft Azure, Google Cloud, TensorFlow.

- **FPGA** – Using oneAPI, Bittware had its application running in days vs. what typically would take several weeks using Verilog or VHDL*.

- And more... 250+ applications developed with oneAPI tools > view catalog.

*Detailed slides per customer are later in deck. Intel does not control or audit third-party data. You should consult other sources to evaluate accuracy. See Notices & Disclaimers for more details.
oneAPI Development Example

ZIB ported *EasyWave* application from CUDA to DPC++ delivering performance across multi-architectures

- Ported EasyWave written in CUDA to Data Parallel C++ efficiently using the Intel® DPC++ Compatibility Tool
- Achieved strong performance across Intel CPU, GPU and FPGA architectures, and within 5% of CUDA performance on Nvidia P100

Visualization of easyWave tsunami simulation application - Courtesy Zuse Institute Berlin (ZIB)

For workloads and configurations visit [www.Intel.com/PerformanceIndex](http://www.Intel.com/PerformanceIndex). Results may vary. Intel does not control or audit third-party data. You should consult other sources to evaluate accuracy.
Bittware

https://www.youtube.com/watch?v=8dNrStoJmWE

Ecosystem Adoption & Support

Training

- Essentials of Data Parallel C++
  - Learn the fundamentals of this language designed for data parallel and heterogeneous computing through hands-on practice in this guided learning path.

- Online webinars & courses, developer guides, sample code

Academia

- oneAPI Centers of Excellence: research, enabling code, curriculum, teaching

Community

- oneAPI open specification, DevMesh innovators, community support forums

Summits & Workshops

- Live & on-demand virtual workshops, community-led sessions

Industry Experts

- Training by leading technical training companies worldwide

Intel® DevCloud

- State-of-the-art software and hardware
  - Intel® oneAPI Toolkits + latest Intel® Xeon® processors, GPUs (integrated & discrete), FPGAs
These organizations support the oneAPI initiative 'concept' for a single, unified programming model for cross-architecture development. It does not indicate any agreement to purchase or use of Intel’s products.

*Other names and brands may be claimed as the property of others.
INTEL EVENT CODE: DEV CLOUD ACCESS
HTTPS://INTEL.LY/3H1GGFV

Devcloud Access code:
oneAPI15DEC
Workshop sign-up process – Step 1 of 9

https://intel.ly/3H1GGfv
Workshop sign-up process – Step 2 of 9
https://intel.ly/3H1GGfv
Workshop sign-up process – Step 3 of 9

Click on the link to verify your email, this should refresh the Browser and lead you to the Sign in page. Sign up with your credentials and you will be directed to the DevCloud registration page.

Action Required

Welcome - we have added a profile for you as a result of your interest in Intel® Developers Zone.

Please retain this e-mail for future reference.

Login ID: 

E-mail Address: 

What you need to do

Please verify your e-mail address by clicking this link or by copying the URL into your browser.

Your password should be protected as confidential. Your use of the password and Intel’s websites are governed by Intel’s Terms and Conditions of Use linked from the bottom of each respective site’s web pages.

Do not close the Browser, verify your email!
Workshop sign-up process – Step 4 of 9

Pls. fill in the form and don’t miss to add the Event code in the highlight section.

oneAPI15DEC

As you register you should receive the email.

“We are excited you chose Intel® DevCloud for oneAPI where you can develop, test, and run your workloads across a range of Intel® CPUs, GPUs, and FPGAs using oneAPI software. Free access. No downloads. No installations. No maintenance. Get Started-
https://devcloud.intel.com/oneapi/get_started/
Workshop sign-up process – Step 5 of 9

WELCOME

Intel® DevCloud is preinstalled with the latest Intel® hardware, frameworks, tools, and libraries.

Read and Accept Terms and Conditions

By accessing this site and the cloud computing services that it provides, you acknowledge and accept the following:

- [ ] Intel DevCloud Access and Software License Agreement
- [ ] Colfax Services Terms

[ ] I, Kavita Aroor, accept these terms.

Submit
Workshop sign-up process – Step 6 of 9
https://devcloud.intel.com/oneapi/get_started/

Scroll down the page to connect with JupyterLab*

Connect with Jupyter* Lab

Connect with Jupyter* Notebook
Use Jupyter Notebook to learn about how oneAPI can solve the challenges of programming in a heterogeneous world and understand the Data Parallel C++ (DPC++) language and programming model.

Launch JupyterLab*

Training Resources

DevCloud Commands
Learn about the features of the compute nodes, data management, and how to submit, query, and delete your jobs.

Introduction to oneAPI and Essentials of Data Parallel C++
Use Jupyter Notebook* to learn about how oneAPI can solve the challenges of programming in a heterogeneous world and understand the Data Parallel C++ (DPC++) language and programming model.
Workshop sign-up process – Step 7 of 9

Launch Server

Server not running

Your server is not running. Would you like to start it?

Launch Server

< oneAPI15DEC>
Welcome to Jupyter Notebooks on the Intel DevCloud for oneAPI Projects!

This document covers the basics of the JupyterLab access to the Intel DevCloud for oneAPI Projects. It is not a tutorial on the JupyterLab itself. Rather, we will run through a few examples of how to use the computational resources available on the DevCloud beyond the notebook.

The diagram below illustrates the high-level organization of the DevCloud. This tutorial explains how to navigate this organization.
Workshop sign-up process – Step 9 of 9

Jupyter notebooks – Introduction

*This path would be updated during the workshop